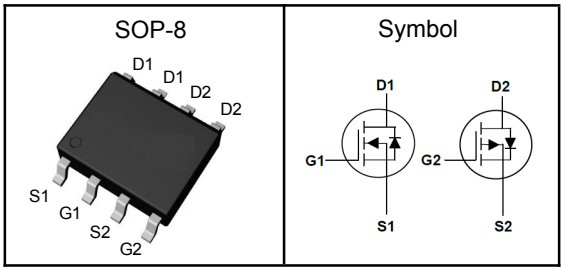
Dual N+P Channel Enhancement Mode MOSFET

Features

- Low Rdson for low conduction loss
- Reliable and Rugged
- ROHS Compliant & Halogen-Free

Pin Description



Applications

- Power Management in Desktop Computer
- DC/DC Converters

V_{DSS}	30	-30	V
$R_{DS(ON)-Typ}$	16	40	mΩ
I_D	7.4	-4.7	A

Absolute Maximum Ratings (T_A=25℃, Unless Otherwise Noted)

Symbol	Parameter	N-Channel	P-Channel	Unit
V_{DSS}	Drain-Source Voltage	30	-30	V
V_{GSS}	Gate-Source Voltage	±20	±20	V
T_J	Maximum Junction Temperature	-55 to 150	-55 to 150	℃
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	℃
I_{DM} ①	Pulse Drain Current Tested	18	-11	A
I_D	Continuous Drain Current	7.4	-4.7	A
P_D	Maximum Power Dissipation	1.6	1.6	W
E_{AS}	Single Pulse Avalanche Energy	15	11	mJ
I_{AS}	Avalanche Current	7.8	-6.8	A

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient[1] (Max)	78	℃/W

Note ① : Max. current is limited by bonding wire.

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150℃.

Note ③ : Surface Mounted on 1in^2 FR-4 board with 1oz.

Dual N+P Channel Enhancement Mode MOSFET

N-Ch Electrical Characteristics (T_J=25℃, Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V	---	---	1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	---	2	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	---	---	±100	nA
$R_{DS(ON)}$	Drain-Source On-state Resistance	V_{GS}=10V, I_D=6.9A	---	16	19	mΩ
		V_{GS}=4.5V, I_D=5A	---	20	26	
gfs	Forward Transconductance	V_{DS}=10V, I_D=1A	---	3.6	---	S
Dynamic Characteristics⑤						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, Freq.=1MHz	---	508	---	pF
C_{oss}	Output Capacitance		---	76	---	
C_{rss}	Reverse Transfer Capacitance		---	60	---	
$T_{d(on)}$	Turn-on Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=6Ω, I_D=1A	---	6	---	nS
T_r	Turn-on Rise Time		---	17	---	
$T_{d(off)}$	Turn-off Delay Time		---	35	---	
T_f	Turn-off Fall Time		---	9	---	
Q_g	Total Gate Charge(4.5V)	V_{DS}=15V , V_{GS}=10V, I_D=7A	---	13	---	nC
Q_{gs}	Gate-Source Charge		---	1.6	---	
Q_{gd}	Gate-Drain Charge		---	2.4	---	
Source-Drain Characteristics						
V_{SD}④	Diode Forward Voltage	V_{GS}=0V , I_S=2A , T_J=25℃	---	0.75	1.2	V
I_S	Continuous Source Current	I_F=5A , di/dt=100A/μs, T_J=25℃	---	8	---	A
I_{SM}	Pulsed Source Current		---	3	---	A

Note ④: Pulse test (pulse width 300us, duty cycle 2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

N-Ch Typical Characteristics

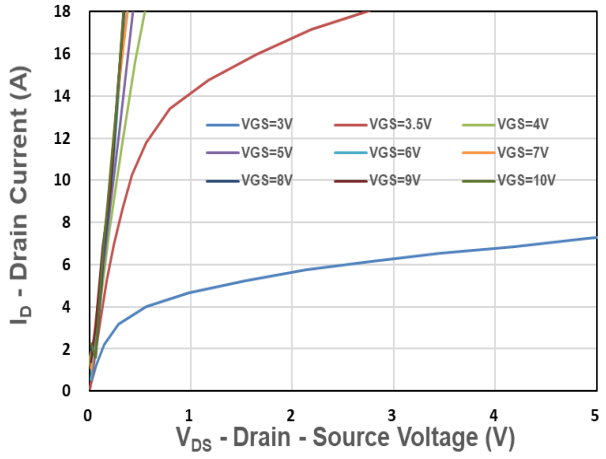


Figure 1. Output Characteristics

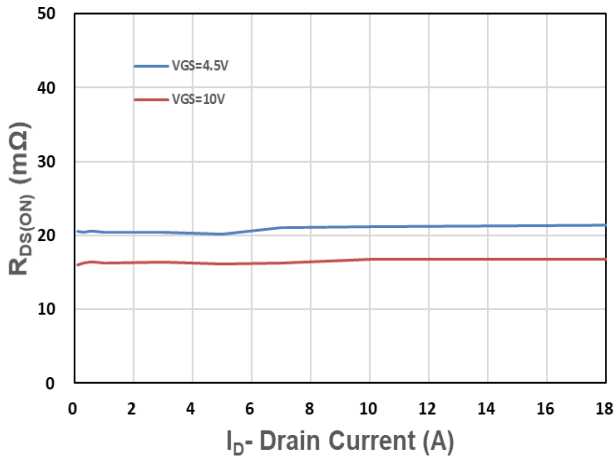


Figure 2. On−Resistance vs. I_D

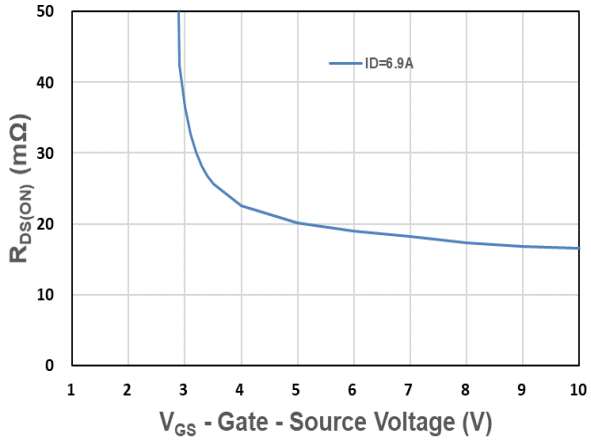


Figure 3. On−Resistance vs. V_{GS}

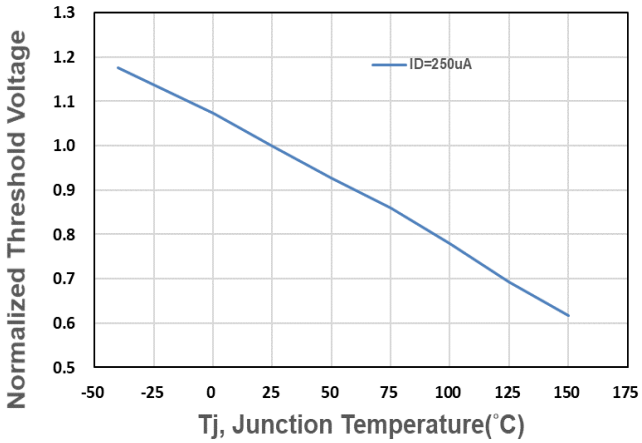


Figure 4. Gate Threshold Voltage

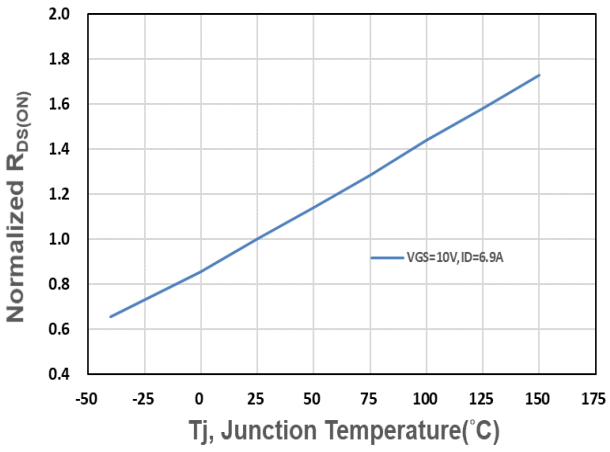


Figure 5. Drain-Source On Resistance

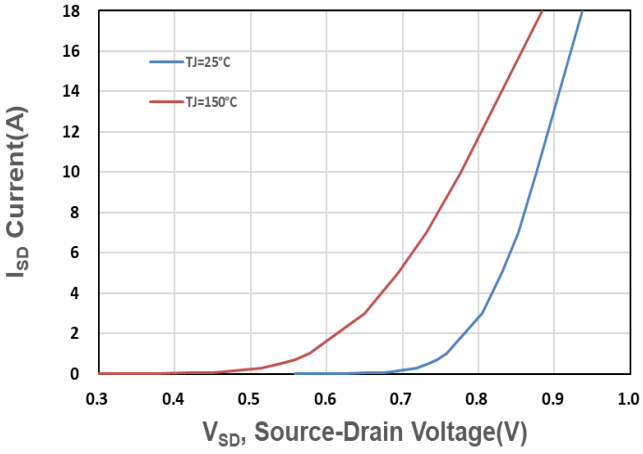


Figure 6. Source-Drain Diode Forward

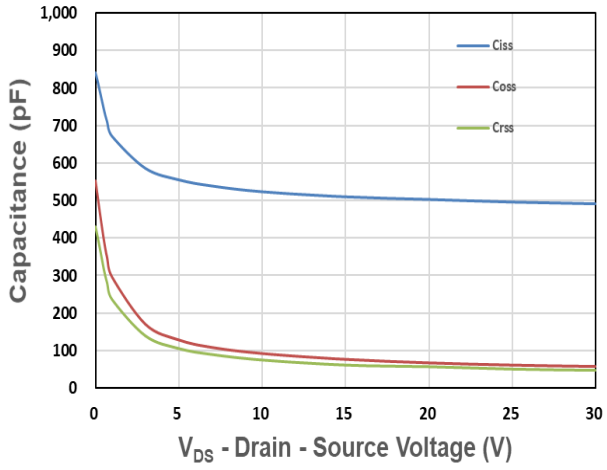


Figure 7. Capacitance

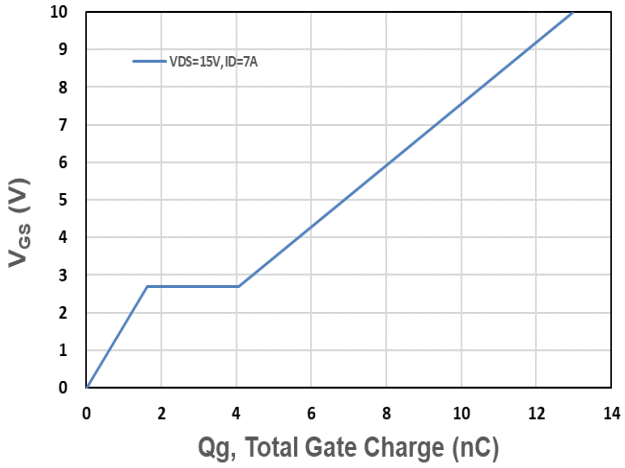


Figure 8. Gate Charge Characteristics

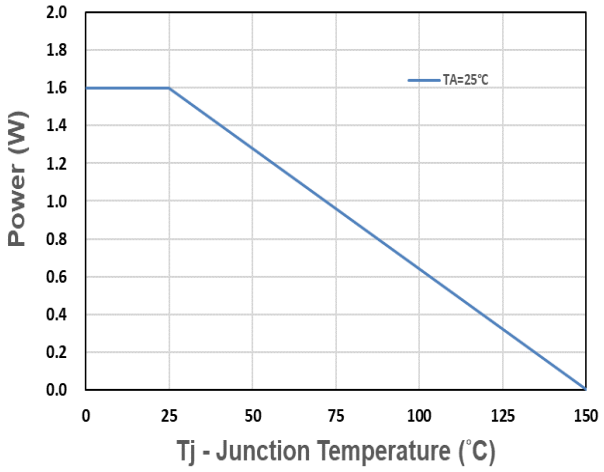


Figure 9. Power Dissipation

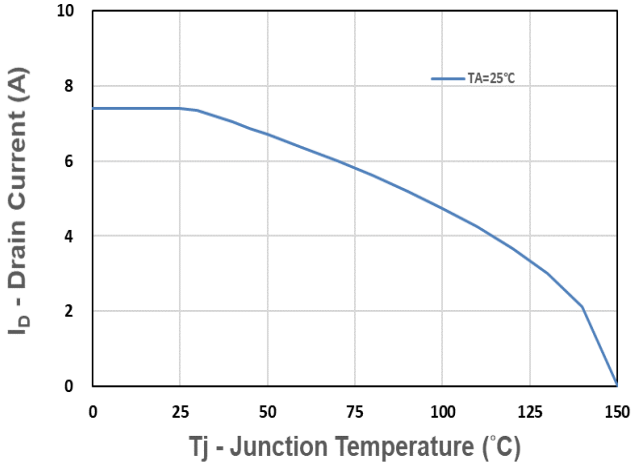


Figure 10. Drain Current

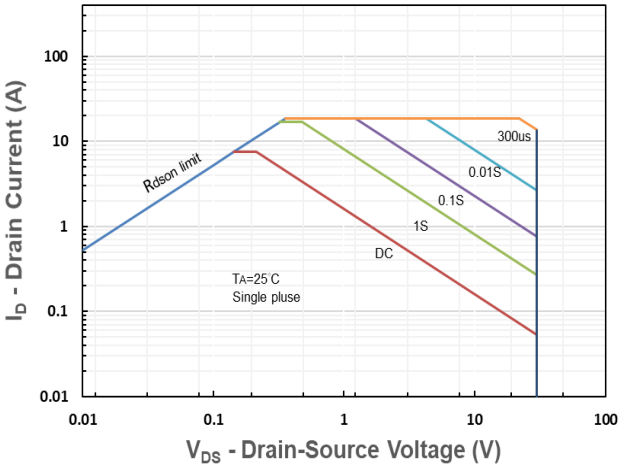


Figure 11. Safe Operating Area

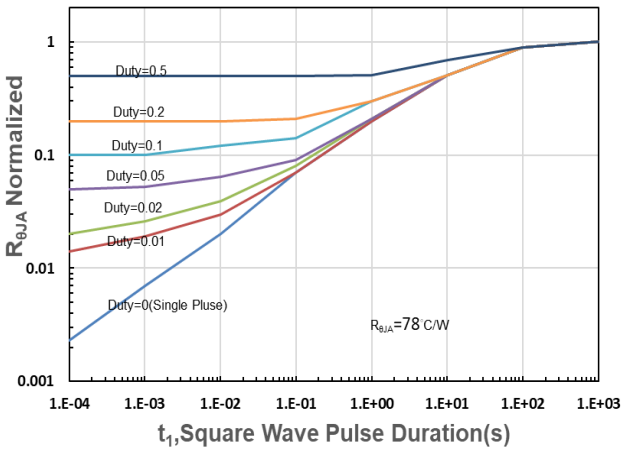


Figure 12. $R_{\theta JA}$ Transient Thermal Impedance

P-Ch Electrical Characteristics (T_J=25℃, Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V	---	---	1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1	---	-2	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	---	---	±100	nA
$R_{DS(ON)}$	Drain-Source On-state Resistance	V_{GS}=-10V, I_D=-5.2A	---	40	48	mΩ
		V_{GS}=-4.5V, I_D=-4A	---	54	71	
gfs	Forward Transconductance	V_{DS}=-10V, I_D=-1A	---	3.7	---	S
Dynamic Characteristics⑤						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, Freq.=1MHz	---	619	---	pF
C_{oss}	Output Capacitance		---	78	---	
C_{rss}	Reverse Transfer Capacitance		---	65	---	
$T_{d(on)}$	Turn-on Delay Time	V_{DD}=-15V , V_{GS}=-10V , R_G=6Ω, I_D=-1A	---	6	---	nS
T_r	Turn-on Rise Time		---	17	---	
$T_{d(off)}$	Turn-off Delay Time		---	65	---	
T_f	Turn-off Fall Time		---	35	---	
Q_g	Total Gate Charge	V_{DS}=-15V , V_{GS}=-10V , I_D=-6A	---	13	---	nC
Q_{gs}	Gate-Source Charge		---	1.3	---	
Q_{gd}	Gate-Drain Charge		---	2.6	---	
Source-Drain Characteristics						
V_{SD}④	Diode Forward Voltage	V_{GS}=0V , I_S=-1.7A , T_J=25℃	---	-0.78	-1.2	V
I_S	Continuous Source Current	I_F=-4.5A , di/dt=100A/μs, T_J=25℃	---	8	---	A
I_{SM}	Pulsed Source Current		---	3	---	A

Note ④: Pulse test (pulse width 300us, duty cycle 2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

P-Ch Typical Characteristics

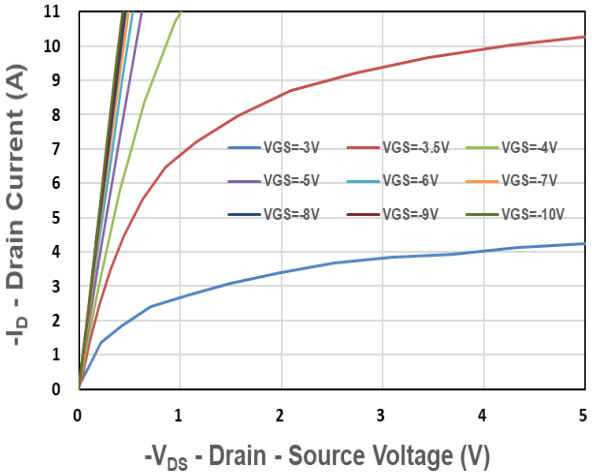


Figure 1. Output Characteristics

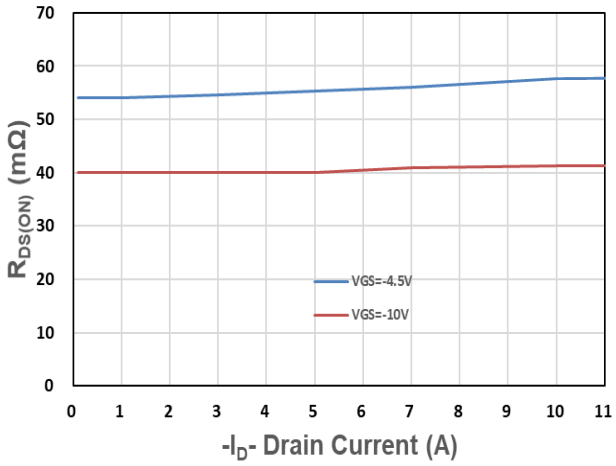


Figure 2. On−Resistance vs. I_D

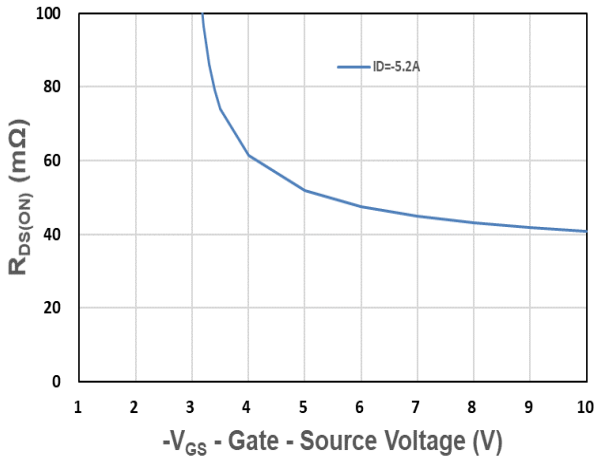


Figure 3. On−Resistance vs. V_{GS}

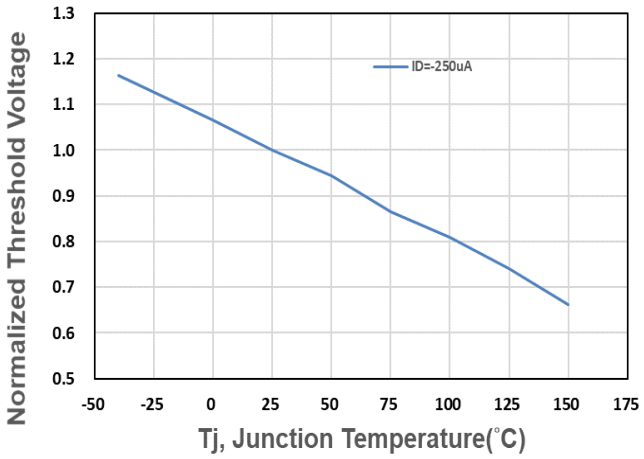


Figure 4. Gate Threshold Voltage

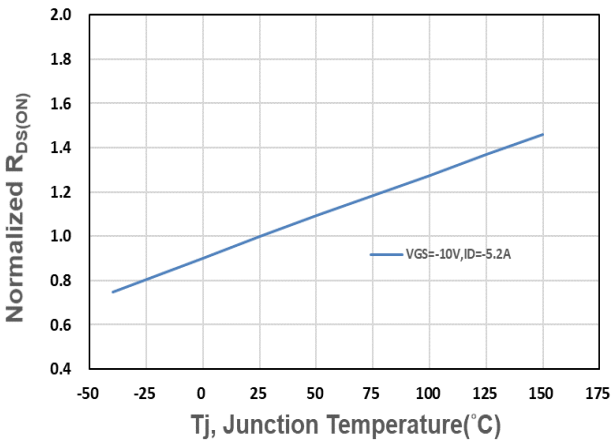


Figure 5. Drain-Source On Resistance

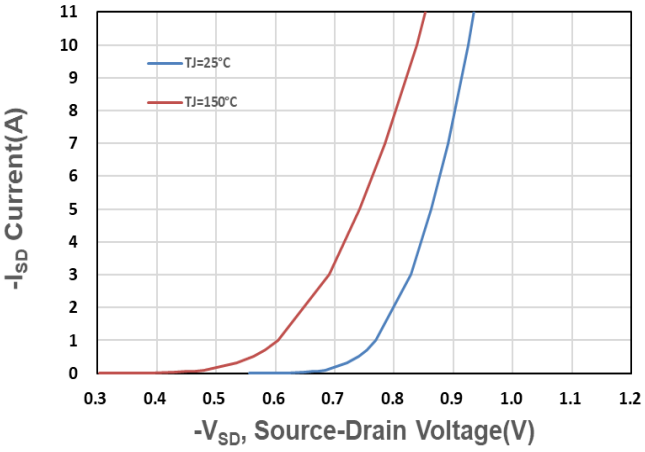


Figure 6. Source-Drain Diode Forward

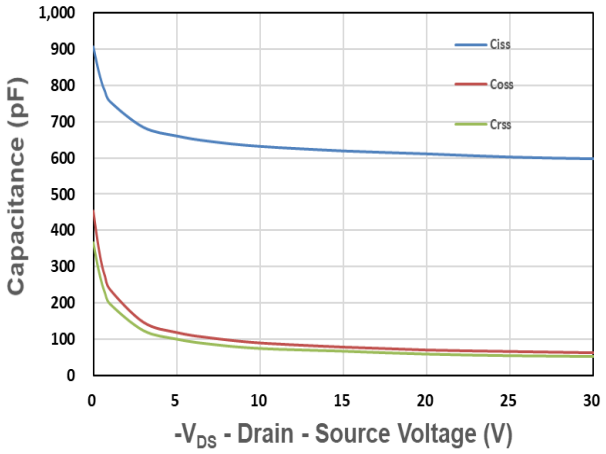


Figure 7. Capacitance

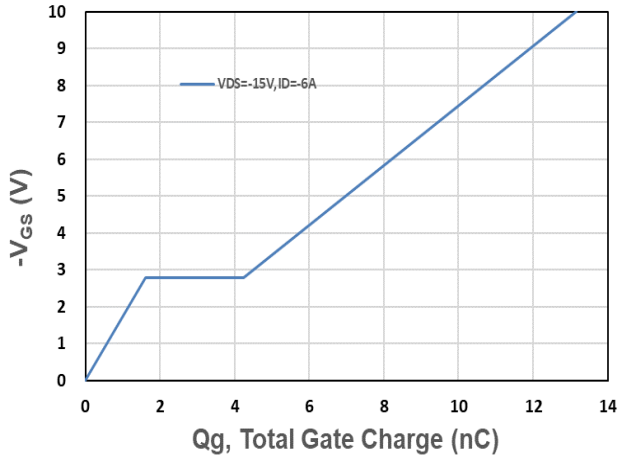


Figure 8. Gate Charge Characteristics

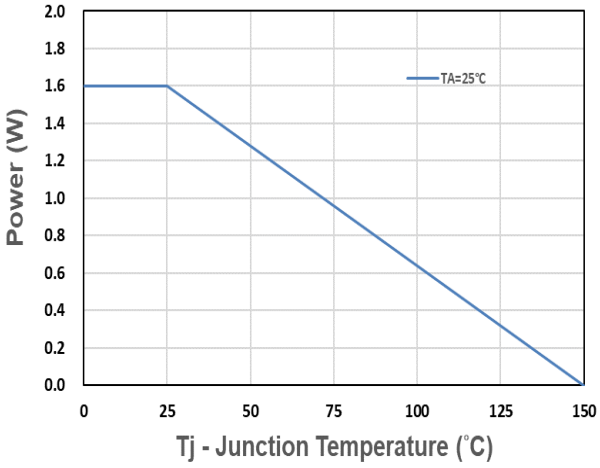


Figure 9. Power Dissipation

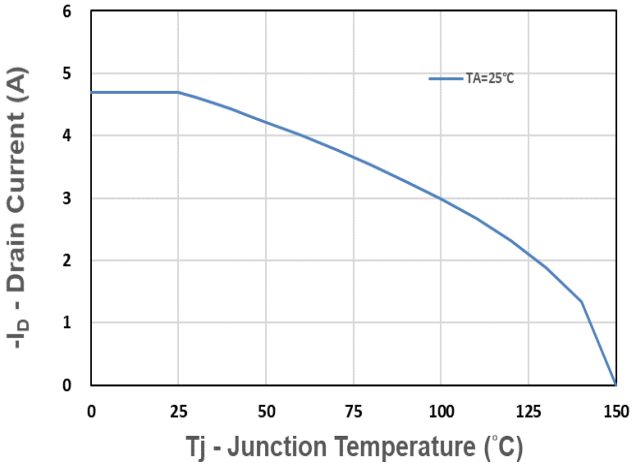


Figure 10. Drain Current

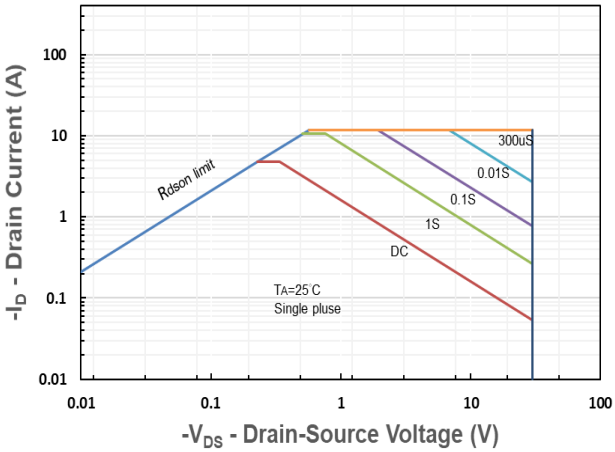


Figure 11. Safe Operating Area

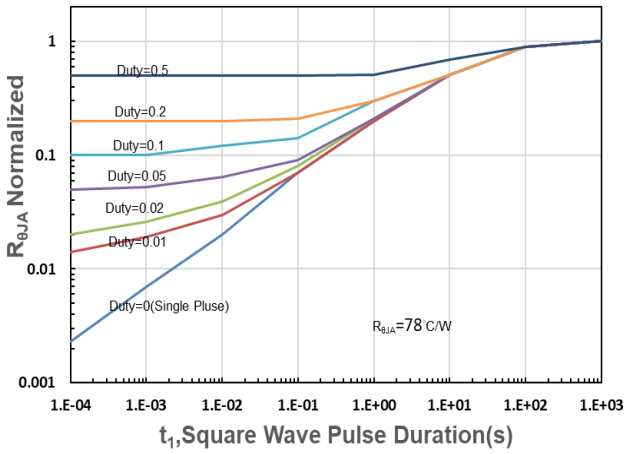
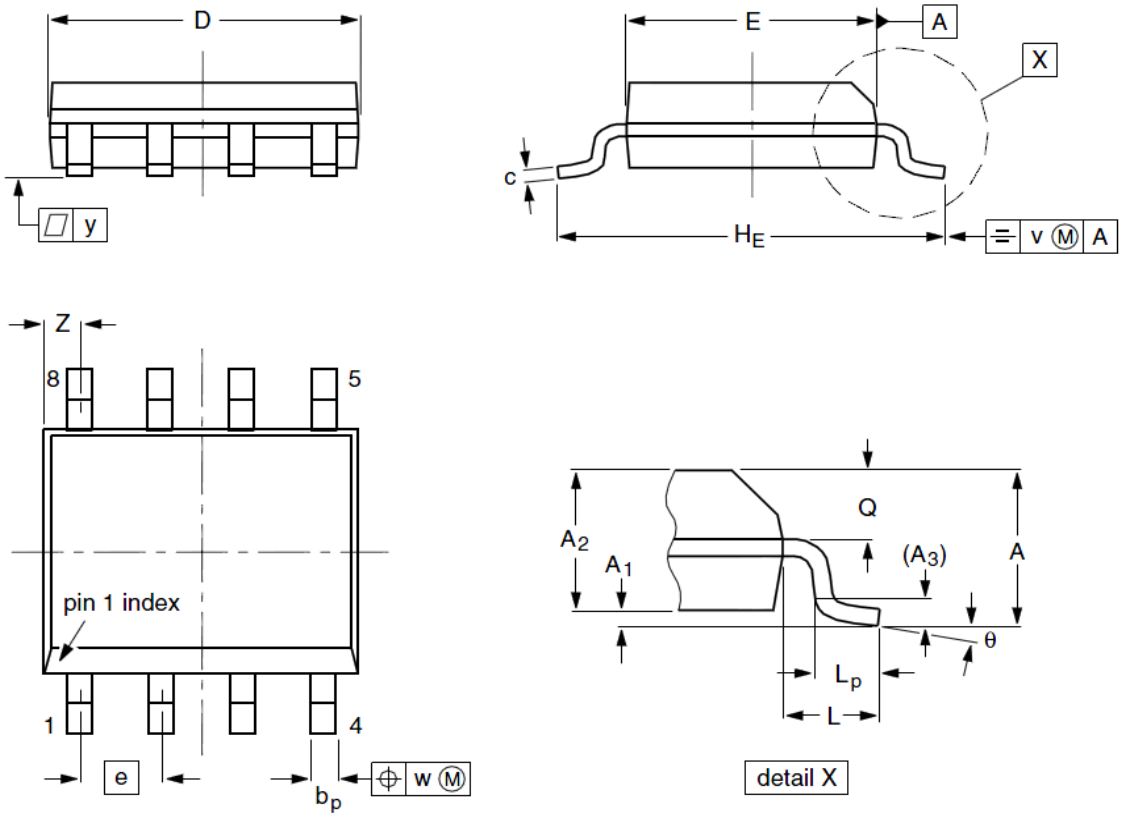


Figure 12. $R_{\theta JA}$ Transient Thermal Impedance

Dual N+P Channel Enhancement Mode MOSFET

SOP-8 Package Outline Dimensions



Symbol	Dimensions (unit:mm)			Symbol	Dimensions (unit:mm)		
	Min	Typ	Max		Min	Typ	Max
A	1.35	1.55	1.75	**A_1**	0.10	0.18	0.25
A_2	1.25	1.45	1.65	**A_3**	--	0.25	--
b_p	0.36	0.42	0.51	**c**	0.19	0.22	0.25
D	4.70	4.92	5.10	**E**	3.80	3.90	4.00
e	--	1.27	--	**H_E**	5.80	6.00	6.20
L	--	1.05	--	**L_P**	0.40	0.68	1.00
Q	0.60	0.65	0.73	**v**	--	0.25	--
w	--	0.25	--	**y**	--	0.10	--
Z	0.30	0.50	0.70	**θ**	0°		8°