

P-Channel Enhancement Mode MOSFET

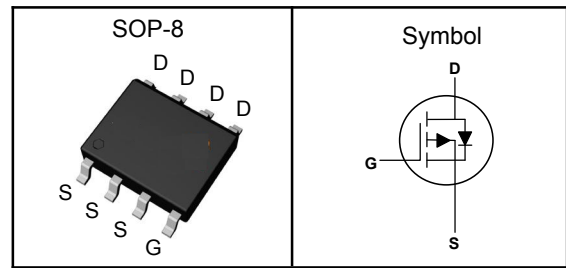
Features

- Low $R_{ds(on)}$ for low conduction loss
- Reliable and Rugged
- ROHS Compliant & Halogen-Free

Applications

- Power Management in Desktop Computer
- DC/DC Converters

Pin Description



V_{bss}	-60	V
$R_{ds(ON)-Typ}$	68	m Ω
I_D	-4.6	A

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	P-Channel	Unit
V_{bss}	Drain-Source Voltage	-60	V
V_{gss}	Gate-Source Voltage	± 20	V
T_J	Maximum Junction Temperature	-55 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$I_{DM}^{①}$	Pulse Drain Current Tested	-18.4	A
I_D	Continuous Drain Current	-4.6	A
P_D	Maximum Power Dissipation	$T_A=25^\circ\text{C}$ 3.1	W

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JA}^{②}$	Thermal Resistance Junction-Ambient ^①	40	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case	24	$^\circ\text{C/W}$

Note ① : Max. current is limited by bonding wire.

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C .

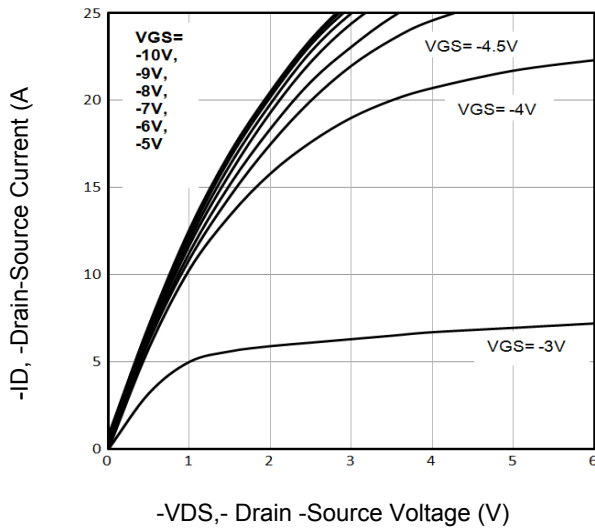
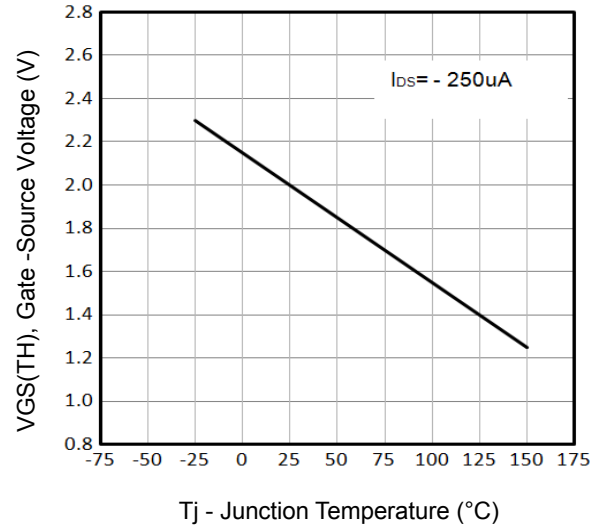
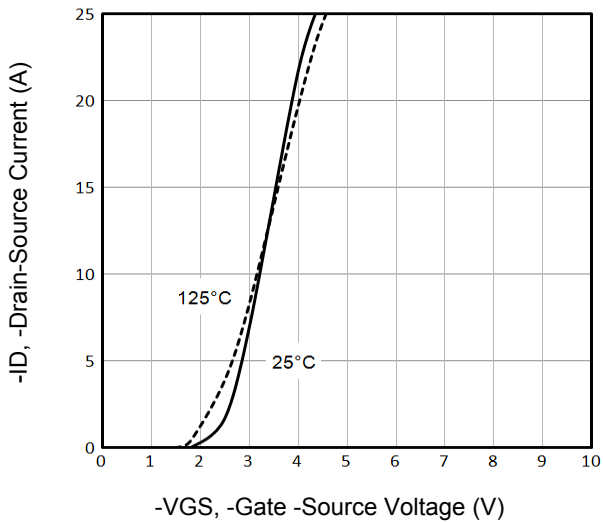
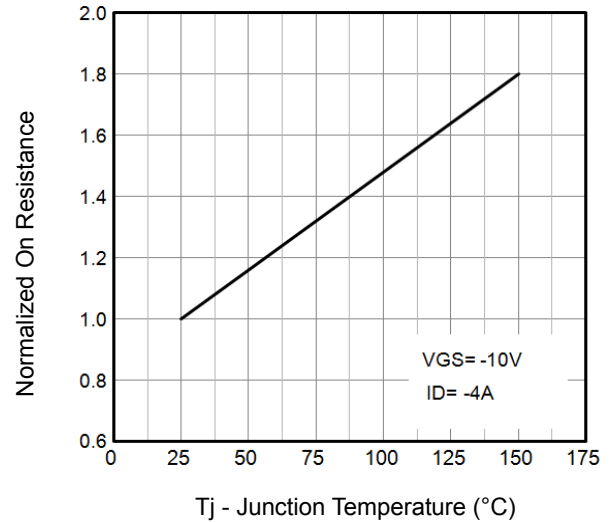
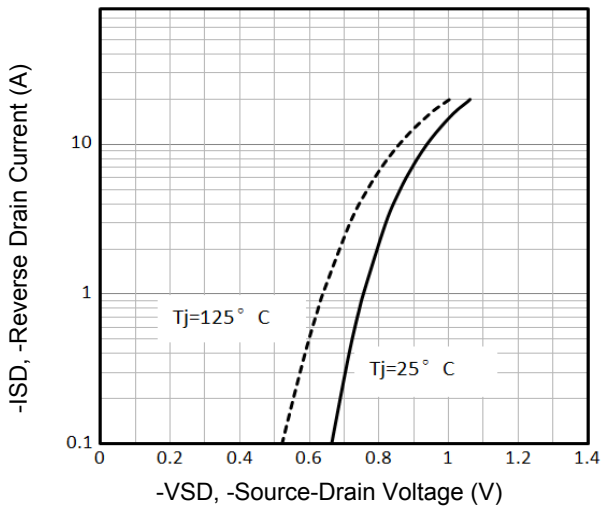
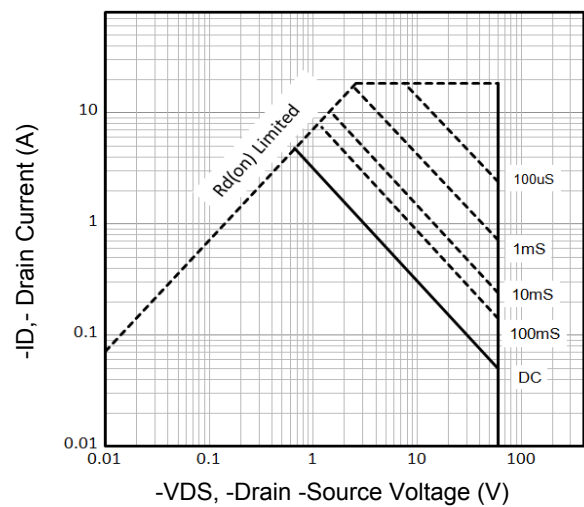
Note ③ : Surface Mounted on 1in^2 FR-4 board with 1oz.

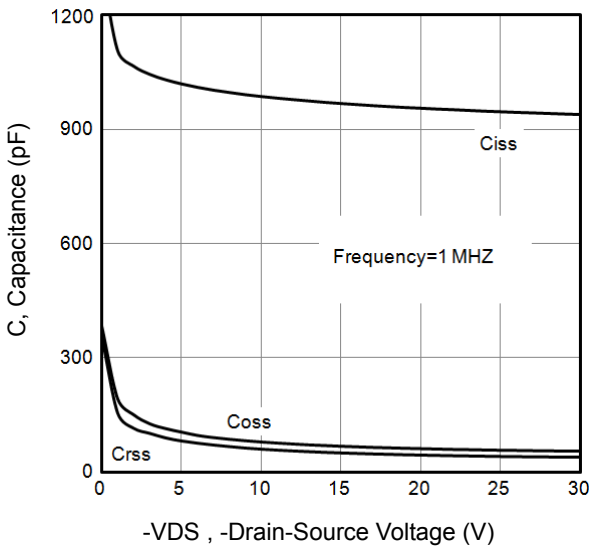
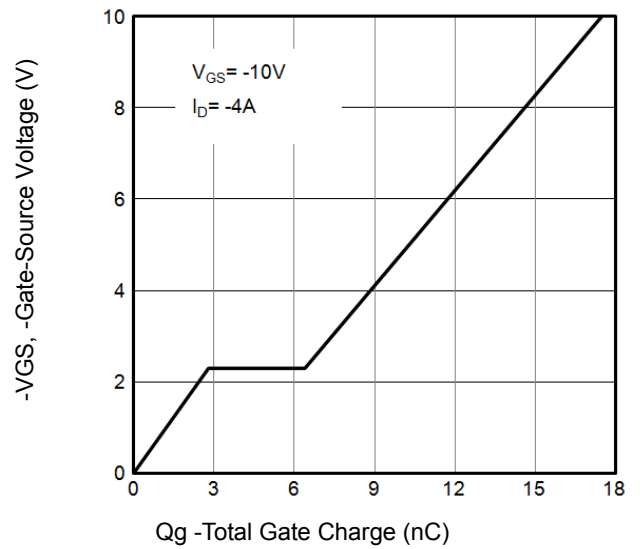
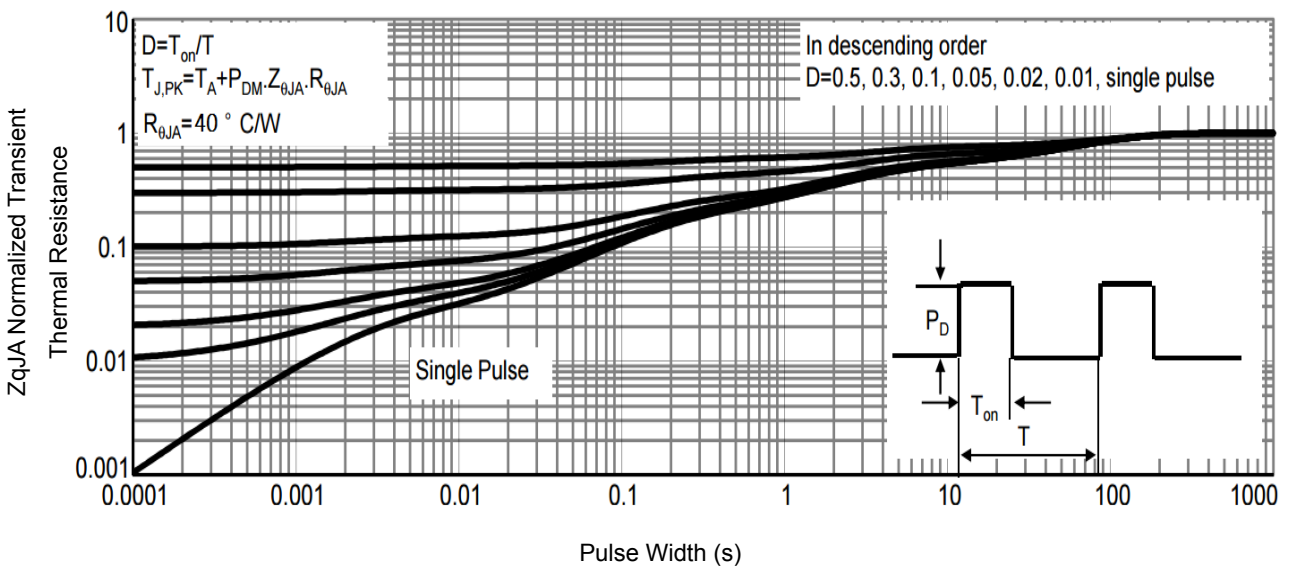
**P-Channel Enhancement Mode MOSFET****Electrical Characteristics** ($T_J=25^\circ\text{C}$, Unless Otherwise Noted)

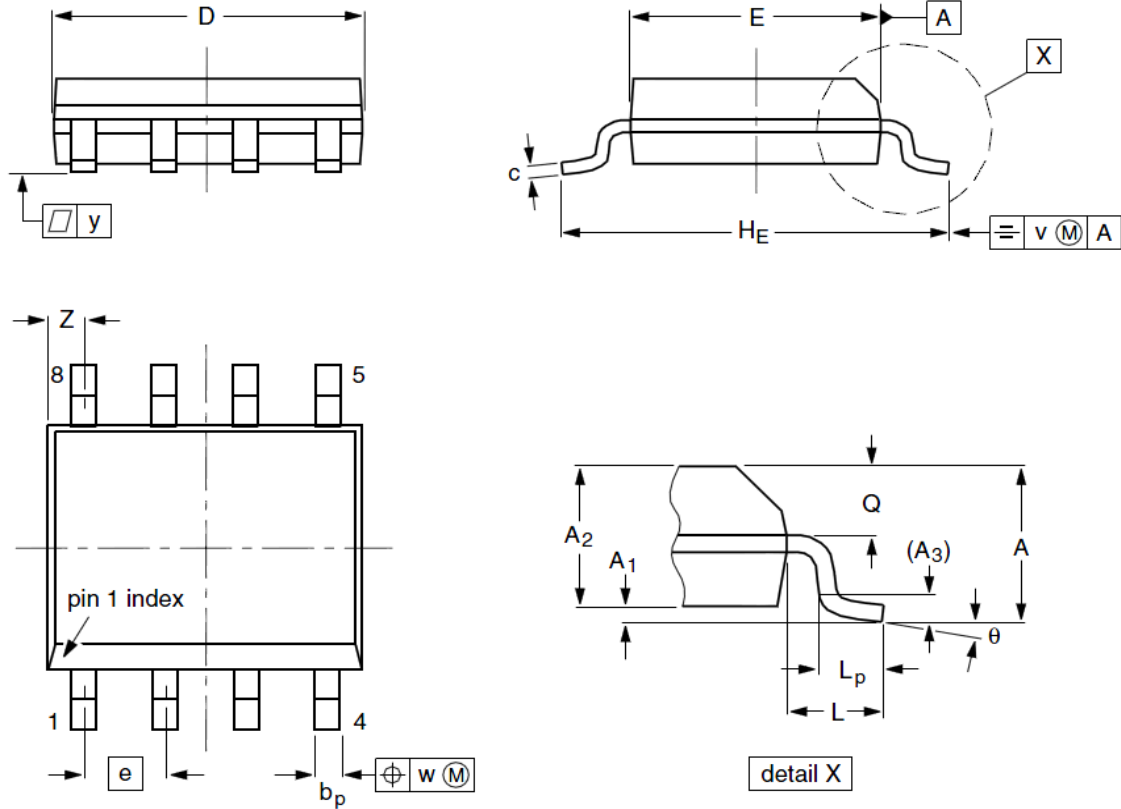
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-60	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-60V, V_{GS}=0V$	---	---	-1	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	---	-3.0	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
$R_{DS(on)}$	Drain-Source On-state Resistance	$V_{GS}=-10V, I_D=-4A$	---	68	90	$m\Omega$
		$V_{GS}=-4.5V, I_D=-2A$	---	80	100	$m\Omega$
Dynamic Characteristics ^⑤						
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=-30V,$ Freq.=1MHz	---	940	---	pF
C_{oss}	Output Capacitance		---	55	---	
C_{rss}	Reverse Transfer Capacitance		---	40	---	
$T_{d(on)}$	Turn-on Delay Time	$V_{DD}=-30V, I_D=-4A,$ $V_{GS}=-10V, R_G=6.8\Omega$	---	9	---	nS
T_r	Turn-on Rise Time		---	4	---	
$T_{d(off)}$	Turn-off Delay Time		---	33	---	
T_f	Turn-off Fall Time		---	8	---	
Q_g	Total Gate Charge	$V_{DS}=-30V,$ $V_{GS}=-10V, I_D=-4A$	---	17.5	---	nC
Q_{gs}	Gate-Source Charge		---	2.8	---	
Q_{gd}	Gate-Drain Charge		---	3.6	---	
Source-Drain Characteristics ($T_J=25^\circ\text{C}$)						
V_{SD}	Diode Forward Voltage _z	$V_{GS}=0V, I_S=-4A, T_J=25^\circ\text{C}$	---	-0.85	-1.2	V
t_{rr}	Reverse Recovery Time	$I_S=-4A,$ $di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	32	---	nS
Q_{rr}	Reverse Recovery Charge		---	39	---	nC

Note ④ : Pulse test (pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$).

Note ⑤ : Guaranteed by design, not subject to production testing.

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Typical Characteristics

Fig1. Typical Output Characteristics

Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

Fig3. Typical Transfer Characteristics

Fig4. Normalized On-Resistance Vs. T_j

Fig5. Typical Source-Drain Diode Forward Voltage

Fig6. Maximum Safe Operating Area

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Fig7. Typical Capacitance Vs. Drain-Source Voltage

Fig8. Typical Gate Charge Vs. Gate-Source Voltage

Fig9. Normalized Maximum Transient Thermal Impedance

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SOP-8 Package Outline Dimensions


Symbol	Dimensions (unit:mm)			Symbol	Dimensions (unit:mm)		
	Min	Typ	Max		Min	Typ	Max
A	1.35	1.55	1.75	A₁	0.10	0.18	0.25
A₂	1.25	1.45	1.65	A₃	--	0.25	--
b_p	0.36	0.42	0.51	c	0.19	0.22	0.25
D	4.70	4.92	5.10	E	3.80	3.90	4.00
e	--	1.27	--	H_E	5.80	6.00	6.20
L	--	1.05	--	L_p	0.40	0.68	1.00
Q	0.60	0.65	0.73	v	--	0.25	--
w	--	0.25	--	y	--	0.10	--
Z	0.30	0.50	0.70	θ	0°		8°